

REMARKS

1 Claims 1-20 have been presented for examination in
2 the above-identified U.S. Patent Application.

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4 Claims 1-20 have been rejected in Office Action
5 dated November 26, 2004, the Office Action imposing a
6 final rejection on all claims.

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8 Claims 1, 8, and 12 have been amended by this
9 Amendment B.

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11 Claim 2 has been cancelled by this Amendment B.

12
13 Claim 21 has been added by this Amendment B.

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15 Claims 1 and 3-21 are in the Application and
16 reconsideration of the Application is hereby respectfully
17 requested.

18
19 Referring to Paragraph No. 6 of Page 2 and
20 continuing through Paragraph 11 on Page 7 of Office
21 Action dated November 26, 2004, Claims 1-20 have been
22 provisionally rejected under the doctrine of obviousness
23 double patenting. As indicated by Examiner, responses to
24 the double patenting rejection, such as the terminal
25 disclaimer, are available. However, because these
26 rejections are provisional, at present, i.e., no Claim
27 having been allowed in either the present Application or
28 the referenced Applications, Applicant prefers to place
29 this matter in abeyance pending the outcome of the
30 prosecution of the Application and/or the references.

1 However, Applicant appreciates the detail provided by
2 Examiner.

3
4 Referring to Paragraph Nos. 10-20, Claims 1-20 have
5 been rejected under 35 U.S.C. 102(b) as being anticipated
6 by U.S. 5,845,153 issued in the name of Sun et al
7 (hereinafter referred to as Sun). Before directly
8 addressing the rejection, the invention disclosed by the
9 Application will be summarized. The Utopia protocol
10 implements a procedure for transferring data between data
11 processing machines. A Utopia-protocol interface is
12 needed to interface between the data processing systems.
13 In the present invention, the Utopia interface interfaces
14 with the direct memory access unit of the processor. The
15 signals defined by the Utopia protocol are given in Table
16 1 on Page 6 and 7 of the Specification. For particular
17 implementations using the Utopia protocol, other signals
18 can be added. For example, the WD-WR and the WRD_RDY
19 signals are shown in Fig. 2 and other Figures of the
20 present Application are not part of the Utopia protocol.
21 In particular, the event signal is disclosed and claimed.
22 This event signal indicating a status of the buffer
23 memory for both the receive and the transmit modes of
24 operation. For the receive mode, the event signal
25 indicates that the buffer memory unit has a complete data
26 cell stored therein. This data cell can then be
27 appropriately redirected through the direct memory unit.
28 For the transmit mode, the event signal indicates to the
29 direct memory access unit that space is available for the
30 storage of an entire data word. This event signal is not
31 a matter of design choice. By signaling the status of the
32 buffer memory unit, the difference between the
33 performance of the direct memory access unit and the
34 buffer memory unit is compensated for. In other words,

1 the extremely rapid direct memory access unit is
2 activated only when a complete data cell can be
3 transmitted. This implementation insures that the
4 activity of the direct memory access unit will not be
5 interrupted once a data transfer is begun. Claims 1, 8,
6 and 12, the independent Claims, have been amended to
7 specifically refer to the event signal. In addition to
8 these limitations, Claims 7, 21 (newly added) and Claim
9 20 describe the clearing of the event signal, the
10 clearing providing an improvement in performance.

11
12 Referring now to the Sun reference, this reference
13 also describes a Utopia-protocol interface for
14 asynchronous transmission of data. The thrust of the
15 disclosure is the segmentation and reassembly of variable
16 data cells. Some signals are described in the Sun
17 reference. For example, in the section cited by
18 Examiner, in Col. 3, lines 1-12, a multi-bit address
19 signal (asserting read or write signal), asserting multi-
20 bit data signal and an address signal are described.
21 Notice that in lines 1-3 of Col. 3, the memory interface
22 addresses an external memory in a conventional manner.
23 While it is not completely clear how this exchange is
24 related to the data exchange of the present invention, it
25 appears that nothing extraordinary, i.e., no new signals,
26 such as the event signal, are employed by the Sun
27 reference. Consequently, the rejection of Claims 1 and
28 3-20 under 35 U.S.C. 102(b) as being anticipated by the
29 Sun reference is respectfully traversed.

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31 In addition, the Claims of the present application
32 include the limitation that the interface unit can act in
33 a master mode or in a slave mode. In certain
34 applications, particularly applications involving digital

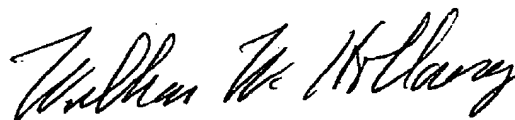
1 signal processors, it is for the interface unit of the
2 present invention to be able to act in either the master
3 mode or the slave mode. The Sun reference does not
4 appear to disclose, teach or suggest this distinction.
5 For this reason also, the rejection of Claims 1 and 3-20
6 under 35 U.S.C. 102(b) as being anticipated by the Sun
7 reference is respectfully traversed.

8
9 Therefore, rejection of Claims 1 and 3-21 under 35
10 U.S.C. 102(b) as being anticipated by the Sun reference
11 is respectfully traversed. In addition, a possible
12 rejection under 35 U.S.C. 103 as being unpatentable in
13 view of the Sun reference would be traversed because the
14 Sun reference does not include features sought to be
15 protected by the claims of the present Application.
16

CONCLUSION

1 In view of the foregoing discussion and the
2 foregoing amendments, it is believed that Claims 1 and 3-
3 21 are now in condition for allowance and allowance of
4 Claims 1 and 3-21 is respectfully requested. Applicants
5 hereby respectfully request a timely Notice of Allowance
6 be issued for this Application.

Respectfully submitted,



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